AMENDMENT TO THE CLAIMS:

This listing of claims will replace all prior versions of claims in the application.

Listing of Claims:

Claims 1-19 cancelled.

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20. (Currently amended) An unpredictable microprocessor or microcomputer comprising:

-a processor ~~(1);~~

-a main memory including an operating system, a main program, and a secondary program;

-a first working memory; ~~(51), a main memory (6) containing an operating system a main program (P1), a secondary program (P2),~~

-a second working memory; ~~(52),~~

-a switching means for switching, while the programs are running, from one of the two working memories ~~(51, 52)~~ to the other working memory, while saving the contents of the two working memories, said switching means comprising access registers associated with each memory including ~~access registers (A1-A3) (D1-D3) associated with each memory (6, 51, 52), said switching means comprising~~ at least one first block of registers ~~(54)~~ for storing the operating context of the programs in the main memory; and,

-a switching circuit ~~(53)~~ for enabling one of the working memories and the access registers ~~(A1-A3)(D1-D3)~~ associated with each memory ~~(51, 52, 6)~~ and controlled by said switching circuit ~~(53)~~.

21. (Currently amended) The unpredictable microprocessor or microcomputer according to claim 20, further including a second block of registers ~~(55)~~ for storing the operating context of the secondary program.

22. (Currently amended) The unpredictable microprocessor or microcomputer according to claim 20, further including means ~~(R1, R2, R3)~~ for de-correlating the running of the programs from an isochronous clock.

23. (Currently amended) The microprocessor or microcomputer according to claim 20, characterized in that the main program can enable or inhibit the switching mechanism or mechanisms by loading the switching circuit ~~(53)~~ for switching and enabling the working memories ~~(51, 52)~~ and blocks of storage registers ~~(54, 55)~~ associated with each respective working memory ~~(51, 52)~~, and storing, respectively, the operating context of the programs in the main memory and the operating context of the secondary program.

24. (Currently amended) The unpredictable microprocessor or microcomputer according to claim 20, characterized in that the second working memory ~~(52)~~ and its access registers ~~(A3, D3)~~ are substituted for the first working memory ~~(51)~~ and its access registers ~~(A2, D2)~~ in utilization by ~~a~~the main program.

25. (Currently amended) The unpredictable microprocessor or microcomputer according to claim 22, characterized in that the de-correlating means comprise a random number generator ~~(2)~~ for triggering, via an interrupt circuit ~~(4)~~, a

random interrupt for desynchronizing the running of the programs in the processor, by randomly jumping to the secondary program ~~(P2)~~.

26. (Currently amended) The unpredictable microprocessor or microcomputer according to claim 23, characterized in that the de-correlating means comprise a time counting system ~~(R3)~~ independent from the processor ~~(1)~~ for, after the time count, triggering an interrupt for returning from the secondary program to the main program.

27. (Currently amended) The unpredictable microprocessor or microcomputer according to claim 23, characterized in that the means ~~(53, 54, 55, A2, A3, D2, D3)~~ for switching working memories is controlled by the processor and its program, by the random interrupt system ~~(2, 4)~~, by a timer ~~(R3)~~, or by any combination of at least two of the three named elements.

28. (Currently amended) The unpredictable microprocessor or microcomputer according to claim 20, characterized in that the means ~~(53, 54, 55, A2, A3, D2, D3)~~ for switching working memories is enabled by being loaded by the processor ~~(1)~~ running a main program sequence.

29. (Currently amended) The unpredictable microprocessor or microcomputer according to claim 20, characterized in that the secondary program ~~(P2)~~ uses a working space identical to that of the main program ~~(P1)~~ in the main memory ~~(6)~~.

30. (Currently amended) The unpredictable microprocessor or microcomputer according to claim 20, characterized in that the secondary program ~~(P2)~~ uses a working space smaller than that of the main program.

31. (Currently amended) The unpredictable microprocessor or microcomputer according to claim 20, characterized in that the switching means carry out the substitution of the memories ~~(51, 52, 53, 54, 55, A2, A3, D2, D3)~~ and the associated contexts within the execution cycle of an instruction from the microprocessor.

32. (Currently amended) The unpredictable microprocessor or microcomputer according to claim 20, characterized in that the secondary program ~~(P2)~~ does not modify the general operating context of the main program ~~(P1)~~ in order to allow the main program to return without having to reestablish said context.

33. (Currently amended) The unpredictable microprocessor or microcomputer according to claim 32, characterized in that the context of the main program ~~(P1)~~ is reestablished either automatically by the secondary program ~~(P2)~~ or automatically by the switching means ~~(53)~~ before returning control to the main program ~~(P1)~~.

34. (Currently amended) The unpredictable microprocessor or microcomputer according to claim 20, characterized in that it further comprises means for substituting the memory of the secondary program ~~(P2)~~ for the memory of the main program ~~(P1)~~.

35. (Currently amended) The unpredictable microprocessor or microcomputer according to claim 20, characterized in that the main program ~~(P1)~~ can use the first working memory ~~(51)~~ and/or the second working memory ~~(52)~~ alternately or simultaneously.

36. (Currently amended) The unpredictable microprocessor or microcomputer according to claim 23, characterized in that loading of the switching circuit ~~(53)~~ makes it possible to mask or unmask de-correlating interrupts.

37. (Currently amended) The unpredictable microprocessor or microcomputer, according to claim 25, characterized in that an interrupt triggered by the secondary program ~~(P2)~~ effects return to the main program ~~(P1)~~ after the switching register ~~(53)~~ has been properly loaded, by executing an instruction of the main program ~~(P1)~~ or the secondary program ~~(2)~~, in order to unmask the interrupts.

38. (Previously added) The unpredictable microprocessor or microcomputer, according to claim 20, characterized in that the microprocessor or microcomputer is embodied in a monolithic integrated circuit.

39. (Currently amended) The ~~Unpredictable~~ unpredictable microprocessor or microcomputer according to claim 21, further including means ~~(R1,R2,R3)~~ of de-correlating the run-through of the programs with respect to an isochronal clock.

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40. (Currently amended) The unpredictable microprocessor ~~Microprocessor~~ or microcomputer according to claim 21 characterized in that the main program is adapted to enable or inhibit the switching mechanism or mechanisms by loading the switching circuit ~~(53)~~ of working memories ~~(51, 52)~~ and of the memorization register blocks ~~(54,55)~~ associated with each respective working memory ~~(51, 52)~~.

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41. (Currently amended) The unpredictable ~~Unpredictable~~ microprocessor or microcomputer according to claim 21 characterized in that the second working memory ~~(52)~~ and the associated access registers ~~(A3,D3)~~ of the second working memory are adapted to be replaced in the use thereof by a main program, with said first memory ~~(51)~~ and the associated access registers ~~(A2,D2)~~ of the first memory.

42. (Currently amended) The unpredictable~~Unpredictable~~ microprocessor or microcomputer according to claim 22 characterized in that the de-correlating means comprise a random generator.

43. (Currently amended) The unpredictable microprocessor~~Microprocessor~~ or microcomputer according to claim 25 characterized in that the means of de-correlation include a time counting system ~~(R3)~~ independent of the processor ~~(1)~~ for enabling, at the end of a time count, the triggering of an interruption to return from the secondary program ~~(P2)~~ to the main program ~~(P1)~~.

44. (Currently amended) The unpredictable~~Unpredictable~~ microprocessor or microcomputer according to claim 25 characterized in that the means of switching ~~(53, 54, 55, A2, A3, D2, D3)~~ the working memories is controlled, either by one of the

microprocessors and the program thereof, the random interruption system ~~(2,4)~~, a time counter ~~(R3)~~, or a combination of at least two out of the three named elements.

45. (Currently amended) The unpredictable microprocessor~~Microprocessor~~ or microcomputer according to claim 22 characterized in that the main program is adapted to enable or inhibit the switching mechanism or mechanisms by loading the switching circuit ~~(53)~~ of working memories ~~(51,52)~~ and of the memorization register blocks ~~(54,55)~~ associated with each respective working memory ~~(51,52)~~.

46. (Currently amended) The unpredictable~~Unpredictable~~ microprocessor or microcomputer according to claim 22 characterized in that the second working memory ~~(52)~~ and the associated access registers ~~(A3,D3)~~ of the second working memory are adapted to be replaced in the use thereof by a main program, with said first memory ~~(51)~~ and the associated access registers ~~(A2,D2)~~ of the first memory.

47. (Currently amended) The unpredictable~~Unpredictable~~ microprocessor or microcomputer according to claim 26 characterized in that the means of switching ~~(53, 54, 55, A2, A3, D2, D3)~~ the working memories is controlled, either by one of the microprocessors and the program thereof, the random interruption system ~~(2,4)~~, a time counter ~~(R3~~, or by a combination of at least two out of the three named elements.

48. (Currently amended) The unpredictable~~Unpredictable~~ microprocessor or microcomputer according to claim 25 characterized in that the interruption circuit ~~(9)~~ triggers the random generator to thereby trigger the random interrupt to desynchronize

execution of the programs in the processor, by random connection to the secondary program ~~(P2)~~.

49. (Currently amended) ~~Unpredictable~~ The unpredictable microprocessor or microcomputer according to claim 26 characterized in that the de-correlation includes a time counting system ~~(R3)~~ independent of the processor ~~(1)~~ for enabling, at the end of a time count, the triggering of an interruption to return from the secondary program ~~(P2)~~ to the main program ~~(P1)~~, and the means of switching ~~(53, 54, 55, A2, A3, D2, D3)~~ the working memories is controlled by one of the microprocessors and the program thereof, the random interruption system ~~(2,4)~~, a time counter ~~(R3)~~ or by a combination of at least two of the three named elements.

50. (Currently amended) The unpredictable~~Unpredictable~~ microprocessor or microcomputer according to claim 21 characterized in that the means of switching ~~(53, 54, 55, A2, A3, D2, D3)~~ the working memories is confirmed by loading from the processor executing a main program sequence.